REMARKS

Reconsideration and allowance of this application are respectfully requested in light of the above amendments and the following remarks.

The Applicants acknowledge with appreciation the indication in the Office Action that claims 11, 14, 16, 17, and 19-21 are allowable. Allowable claims 11, 14, 16, 17, and 19-21 have been rewritten in independent form to include all limitations of base claim 1 and any intervening claims as new claims 25-31. Claims 25-31 have been drafted to avoid the issue underlying the objection applied to claim 11 in Section 4 of the office action. Therefore, allowance of claims 25-31 is deemed to be warranted.

Claims 1, 3, and 7 have been amended, and claims 2, 6, 11, 14, 16, 17, and 19-23 have been canceled. Claims 24-33 have been newly added. Claim 1 now incorporates the subject matter of canceled claim 2, and claim 24 recites the subject matter of canceled claim 6 in independent form. Claims 32 and 33 recite the subject matter of amended claim 1 and canceled claims 22 and 23 in independent form. New claims 32 and 33 have been drafted to avoid the issues underlying the objections applied to claims 22 and 23 in Section 5 of the office action.

Claims 1-4, 6-10, 12, 13, and 15 were rejected, under 35 USC 102(b), as being anticipated by Suemura et al. (US 5,687,181). Claim 5 was rejected, under 35 USC § 103(a), as being unpatentable over Suemura in view of Frederickson (US 6,105,159). Claim 18 was rejected, under 35 USC § 103(a), as being unpatentable over Suemura in view of Watanabe et al. (US 4,965,576). To the extent these rejections may be deemed applicable to the amended claims, the Applicants respectfully traverse based on the points set forth below.

Claim 1 now recites the limitations of original claim 2 and defines an encoding method that encodes an information bit sequence using two separate encoding operations. In a first encoding operation, the information bit sequence is separated into code block segments and each segment is individually encoded. In a second operation, the information bit sequence as a whole is encoded.

By contrast to the claimed subject matter, Suemura discloses, in Figs. 3 and 4, dividing a 64 bit data sequence into 16 parallel data sequences of 4 bits each (i.e., 64 bits/16 sequences = 4 bits/sequence) (see Suemura col. 4, lines 57-61, and col. 6, lines 43-47). Each of the 16 parallel data sequences is separately encoded by an encoder 11 (see col. 4, lines 61-65, and col. 6, lines 47-52).

Suemura does not disclose encoding the entire 64 bit data sequence as one code block in a separate encoding operation from those used to encode the 16 code block groups of 4 bits distributed from the 64 bit data sequence. Thus, Suemura does not disclose the claimed subject matter of both: (1) encoding an information bit sequence as one code block in a first encoding operation and (2) separating the information bit sequence into multiple code blocks and individually encoding each of the multiple code blocks in a second encoding operation.

Accordingly, the Applicants respectfully submit that Suemura does not anticipate the subject matter now defined by claim 1. Independent claims 32 and 33 similarly recite the above-mentioned subject matter distinguishing method claim 1 from Suemura, but are apparatus claims. Therefore, the rejections applied to claims 5 and 18 are considered to be obviated, and allowance of claims 1, 32, and 33 and all claims dependent therefrom is deemed to be warranted.

New claim 24 recites the subject matter of original claim 6 in independent form and defines an encoding method that separates an information bit sequence into multiple code block segments and encodes each segment using a different encoding method.

By contrast to the claimed subject matter, Suemura discloses, in Fig. 4, dividing a 64 bit data sequence into 16 parallel data sequences of 4 bits each (i.e., 64 bits/16 sequences = 4 bits/sequence) (see Suemura col. 6, lines 43-47). Each of the 16 parallel data sequences is separately encoded by a Reed Solomon encoder 11 (see col. 6, lines 47-52). Thereafter, eight encoders 8B10B each receives two of the 16 parallel Reed Solomon encoded data sequences and encodes the two data sequences (see col. 6, lines 52-63).

Although Suemura discloses applying two separate (and possibly different) encoding operations to the same data sequence, Suemura does not disclose applying a different encoding method to each of multiple data sequences, as recited in claim 24. Instead, Suemura applies the same Reed Solomon encoding method to each of 16 parallel data sequences, and after 8 groups of 2 Reed Solomon encoded parallel data sequences are formed, Suemura applies the same 8B10B encoding method to each of the 8 groups of data sequences. Thus, each of Suemura's 16 parallel data sequences receives identical Reed Solomon encoding and identical 8B10B encoding. As a result, Suemura does not disclose the claimed subject matter of separating an information bit sequence into a plurality of code block segments and encoding each of the code block segments using a different encoding method.

Accordingly, the Applicants respectfully submit that Suemura does not anticipate the subject matter defined by claim 24. Therefore, allowance of claim 24 is considered to be warranted.

In view of the above, it is submitted that this application is in condition for allowance, and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,

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